# P.E.S. COLLEGE OF ENGINEERING, MANDYA – 571401



## (An Autonomous & Govt. Aided Institution, Affiliated to VTU, Belagavi)

An Internship Report

**On**

# “SYNOPSYS INTER INTEGRATED (I2C) PROTOCOL CIRCUIT DESIGN AND VERIFICATION USING VERILOG”

***S*u*bmitted in partial fulfilment for the award of the degree of***

## BACHELOR OF ENGINEERING

**In**

## ELECTRONICS AND COMMUNICATION ENGINEERING

***Submitted by***

## SOHANA MV 4PS22EC156

*Internship Carried Out*

*At*

## RJ SEMICONDUCTORS

### Under the guidance of

### M SUBRAMANYAM

**Associate Professor**

## DEPARTMENT OF ELECTRONICS AND COMMUNICATION

**ENGINEERING 2023-24**

**P.E.S. COLLEGE OF ENGINEERING, MANDYA**



**(An Autonomous & Govt. Aided Institution, Affiliated to VTU, Belagavi)**

## Department of Electronics and Communication Engineering

**CERTIFICATE**

This is to certify that **SOHANA MV** bearing USN **4PS22EC156** has successfully completed the **Internship-I** work (P22INT408) entitled “**Synopsys inter integrated circuit (I2C)protocol design and verification using verilog**” carried out at **RJ Semiconductors** in partial fulfilment for the award of Degree of **Bachelor of Engineering in Electronics and Communication Engineering, P.E.S. College of Engineering, Mandya** (An Autonomous Institution Affiliated to VTU, Belagavi) during the academic year **2023-2024**. It is certified, that all corrections suggested have been incorporated in the report deposited in the library. The Internship has been approved as it satisfies the academic requirements in respect of Internship work prescribed for the Degree in Bachelor of Engineering.

|  |  |  |
| --- | --- | --- |
| Signature of the Mentor | Signature of the HOD | Signature of Principal |
| M Subramanyam | Dr. Punith Kumar M B | Dr. H M Nanjundaswamy |
| Associate professor | Professor & HOD | Professor and Principal |

|  |  |  |  |
| --- | --- | --- | --- |
| **Details of Internship report Viva Voce Examination** | | | |
| **Sl.**  **No.** | **Name of the Examiners** | **Signature** | **Date** |
| **1** |  |  |  |
| **2** |  |  |  |



# P.E.S COLLEGE OF ENGINEERING, MANDYA - 571401

(An Autonomous Institution Affiliated to VTU, Belagavi)

Department of electronics and communication engineering

# DECLARATION

This is declared that, **SOHANA MV**- **4PS22EC156,** named students of 4th semester B.E Department of Electronics and Communication Engineering, P.E.S College of Engineering, Mandya, have successfully completed Internship-I work on **“Synopsys inter integrated circuit (I2C) protocol design and verification using verilog”** and completed work entitled under the guidance of **M SUBRAMANYAM** Assistant Professor, Department of Electronics and Communication Engineering P.E.S College of Engineering, Mandya. The Project report of the same is submitted in partial fulfilment of the requirement for the award of **Bachelor of engineering degree in Department of Electronics and Communication Engineering affiliated to Visvesvaraya Technological University, Belagavi** during the year 2023-2024.

Date: - 06-08-2024

Place: -Mandya

## ACKNOWLEGDEMENT

The satisfaction that accompanies the successful completion of the internship I report which would be complete only with the mention of the lecturer’s who the part of this course was.

We are grateful to **P. E. S COLLEGE OF ENGINEERING, MANDYA** for providing us an opportunity to enhance our knowledge through the internship program.

We would like to express profound thanks to our mentor **M SUBRAMANYAM** Assistant Professor, Department of Electronics and Communication Engineering for the keen interest and encouragement in our internship program.

We express our sincere thanks to **Dr. H M NANJUNDASWAMY** Principal, PESCE - Mandya for providing an opportunity and means to complete this program.

We express our heart full thanks to **Dr. PUNITH KUMAR M B**, Associate Professor and Head of the Department of Electronics and Communication Engineering, PESCE - Mandya for encouragement in our spirit, whose cooperation and guidance helped in nurturing this.

## ABSTRACT

The project focuses on the development of a Synopsys inter integrated circuit (I2C) protocol design and verification using Verilog Hardware Description Language (HDL). I2C is serial communication protocol. It is used to establish connection from one block to another block outside the chip. This control chip aims to enhance the inter integrated circuits efficiency, reliability, and user experience by incorporating sophisticated features such as power efficiency, data rate, low pin count and master or slave functionality. The chip's architecture is designed using two signals serial data line (SDA) and serial clock line (SCL). The control system integrates several key components: Transfer of data through SDA, write operation and read operation.

First, the address and data are transferred to I2C through the SDA pin bit by bit. Then, the write and read operation takes place as per the design. Verilog HDL is used to design and simulate the chip, leveraging its capabilities to model the hardware at various abstraction levels. The project involves creating detailed behavioral and structural models, performing synthesis, and implementing the chip on an FPGA (Field Programmable Gate Array) for testing and validation. Through this project, we aim to demonstrate the feasibility and advantages of using Verilog HDL for developing a inter integrated circuit. The implementation showcases the potential for increased functionality, better user interaction, and improved operational efficiency in inter integrated circuits. The project's outcomes could contribute significantly to the I2C industry, offering a robust solution for managing and operating inters integrated circuits. The Verilog code for these inter integrated circuit is synthesized and simulated using Questa Sim 64, one of the powerful simulation tools for verifying HDL designs. The simulation results demonstrate the correct functionality of the I2C protocol, including simultaneous read/write operations, data integrity, and timing accuracy. The design is verified through extensive test benches that cover various scenarios, ensuring all the input conditions

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## CHAPTER 1

**ABOUT THE COMPANY**

RJ Semiconductor is a specialized training institute focused on providing advanced courses in VLSI (Very-Large-Scale Integration) technology, SOC (System on Chip) design, and functional verification. Their mission is to enhance the expertise of their students through hands-on training programs that are endorsed by industry leaders.

RJ Semiconductor is an esteemed training institute specializing in advanced VLSI (Very- Large-Scale Integration) technology, SOC (System on Chip) design, and functional verification. Established with a mission to elevate technical expertise, the institute offers hands-on courses endorsed by industry leaders, unlocking numerous opportunities in the semiconductor field.

The institute's curriculum includes a variety of comprehensive courses such as AMBA protocol training, SOC training, and internships in advanced VLSI design and verification. These programs are designed to provide practical, job-oriented skills essential for success in the semiconductor industry. Students gain in-depth knowledge of ARM technologies, VLSI design flow, and SOC architecture, which are crucial for roles in designing Smartphone SOCs, IoT MCUs, and wearable devices.

RJ Semiconductor prides itself on several key features that enhance the learning experience. These include 24/7 lab access, personalized mentoring, mock interviews, and technical group discussions. The institute has a proven track record of excellence over the past five years, offering a 100% job-oriented curriculum that culminates in an internship certificate.

Located in Bangalore, RJ Semiconductor is dedicated to preparing its students for the competitive semiconductor industry through rigorous training and real-world projects guided by industry experts. This comprehensive approach ensures that graduates are well-equipped to meet the demands of leading semiconductor companies.

The objective of RJ Semiconductor is to empower individuals with advanced knowledge and practical skills in the semiconductor industry through comprehensive training programs. The company focuses on:

1. **Elevating Expertise**: Providing hands-on courses endorsed by industry leaders to help students gain a deep understanding of semiconductor technologies and design methodologies.
2. **Job Readiness**: Ensuring students are well-prepared for employment through job- oriented courses, practical lab exercises, and real-world projects.
3. **Comprehensive Training**: Offering a range of courses covering essential topics such as VLSI technology, SOC architecture, AMBA protocols, and functional verification to provide a holistic education.
4. **Support and Development**: Facilitating one-on-one mentoring, mock interviews, and technical group discussions to support students' professional growth and confidence.
5. **Industry Relevance**: Keeping the curriculum aligned with the latest industry standards and technological advancements to ensure graduates are competitive in the job market.



## CHAPTER 2

**SCHEDULE OF TRAINING AND INTERNSHIP**

Training Program: VLSI Design and verification

The training schedule for Fourth-semester students with RJ Semiconductors isas follows:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **DAY** | **TOPIC** | **LEARNING OBJECTIVE** | **CATEGORY** | **HOURS** |
| Monday, 24 June 2024 | VLSI  Flow | Introduction on VLSI flow, Industry demand, Future of VLSI. | Delivery | 2 |
| Digital electronics | Delivery | 4 |
| Tuesday, 25 June 2024 | Digital design | Digital design byusing Basic Gates | Delivery | 2 |
| Digital design  Applications(Combinational and Sequential circuits) | Delivery | 4 |
| Wednesday, 26 June 2024 | Verilog | Verilog Design and Test bench flow ,verilog data types, Procedural Blocks | Delivery | 2 |
| Verilog operators and Verilog loops | Delivery | 4 |
| Thursday 27 June 2024 | verilog | Verilog Case Statements(casex and casez),Blocking and Non Blocking assignments, | Delivery | 2 |
| Race conditions, Setup time and  Hold time ,Task and Functions, Parallel threads | Delivery | 4 |
| Friday ,  28 June 2024 | Verilog | Verilog lab section on Basics of Verilog | Hands on | 2 |



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Saturday 29 June 2024 | Verilog projects | Design of 1KB RAM and ROM then verify using Verilog TB | Hands on | 3 |
| Design of electric vehicle  digital lock system using Verilog | Hands on | 3 |
| Monday, 1 july2024 | Verilog projects | Design of multiple product vending machine | Delivery | 2 |
| Test bench development | Hands on | 4 |
| Tuesday, 2 July2024 | Verilog | Projects lab section | Hands on | 2 |
| Projects lab sections | Hands on | 4 |
| Wednesday, 3 July 2024 | System On Chip | Design SOC AMBA interface using Verilog | Delivery | 2 |
| Test bench development | Hands on | 4 |
| Thursday, 4 July2024 | Verilog | Design of traffic light controller | Hands on | 2 |
| Revision and Interview preparation | Delivery | 4 |



## CHAPTER 3 TASK PERFORMED

* 1. **Problem Statement**

Synopsys inter integrated circuit (I2C) protocol design and verification using verilog.

## Problem Description

Objective:

The Digital Blocks DB-I2C-MS-APB Controller IP Core interfaces a microprocessor via the AMBA APB Bus to an I2C Bus in Standard-Mode. The I2C is a two-wire bidirectional interface standard (SCL is Clock, SDA is Data) for transfer of bytes of information between two or more compliant I2C devices, typically with a microprocessor behind the master controller and one or more slave devices. The DB-I2C-MS-APB is a Master/Slave I2C Controller that in Master Mode controls the Transmit or Receive of data to or from slave I2C devices while in Slave Mode allows an external I2C Master device to control the Transmit or Receive of data.

Methodology:

* + 1. Physical Layer  wiring: I²C typically uses two bi-directional lines, the Serial Data Line (SDA) and the Serial Clock Line (SCL), to transfer data between devices. Both lines are open-drain and require pull-up resistors.  Bus Configuration: It supports multi-master, multi- slave, single-ended communication, meaning multiple masters and slaves can share the bus without conflicts.
    2. Addressing  7-bit and 10-bit Addressing: I²C devices are identified by a unique address. Standard I²C uses 7-bit addressing, allowing up to 127 devices on the bus. However, 10-bit addressing is also supported for a larger number of devices.  Address Frame: Communication begins with the master sending a start condition followed by a 7-bit address and a read/write bit, indicating whether the master intends to write to or read from the slave.
    3. Data Transfer  Start and Stop Conditions: Data transfer is initiated with a start condition (SDA line transitions from high to low while SCL is high) and terminated with a stop condition (SDA line transitions from low to high while SCL is high).  Data Frames: After

the address frame, data is transferred in 8-bit packets. Each data byte is followed by an acknowledgment (ACK) bit from the receiver. If the receiver does not acknowledge, the master can end the transmission with a stop condition.  Acknowledge Bit: After each byte, the receiving device must send an ACK bit to confirm receipt. If an ACK is not received, it indicates an issue, and the master may condition.

* + 1. Clock Synchronization  Clock Stretching: The slave device can hold the SCL line low to pause the master device, allowing time for processing before continuing the data transfer. This is known as clock stretching.
    2. Communication Modes  Master-Slave Communication: The master initiates communication, while the slave responds to the master's requests. The master controls the clock (SCL line), while both master and slave can drive the data (SDA line).  Multi-Master Arbitration: In systems with multiple masters, the I²C protocol has an arbitration mechanism to prevent data collisions. Masters monitor the bus and back off if they detect another master is transmitting.
    3. Error handling  NACK (Not Acknowledged): If a slave device cannot process the data, it sends a NACK bit instead of an ACK bit. The master can then terminate the communication.
       - Bus Monitoring: Devices monitor the bus to ensure proper communication. If an error is detected, such as an unexpected stop condition, the devices can reset their communication state.
    4. High-Speed Mode (Hs-mode)  Fast and High-Speed Modes: Standard I²C operates up to 100 kHz (Standard-mode) and 400 kHz (Fast mode). High-speed mode (Hs-mode) allows speeds up to 3.4MHz, achieved by specific signaling sequences and master clock control.

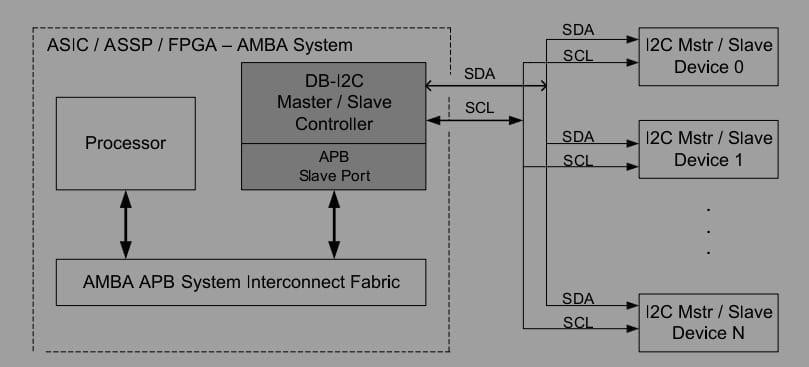
### Deliverables:

1. **Verilog Code:** Well-documented source code for all modules.
2. **Test benches:** Detailed test cases to validate each module and the entire system.
3. **Simulation Results:** Waveforms and logs demonstrating the correct operation of the I2C system.
4. **Documentation:** Comprehensive documentation outlining the design, implementation, and testing processes.



## Design and Development of Solution

Fig: Block Diagram

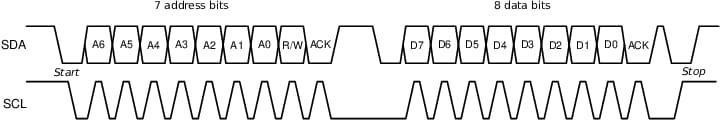


I2C is serial communication protocol. It is used to establish connection from one block to another block outside the chip. This control chip aims to enhance the inter integrated circuits efficiency, reliability, and user experience by incorporating sophisticated features such as power efficiency, data rate, low pin count and master or slave functionality. The chip's architecture is designed using two signals serial data line (SDA) and serial clock line (SCL). The control system integrates several key components: Transfer of data through SDA, write operation and read operation. First, the address and data are transferred to I2C through the SDA pin bit by bit. Then, the write and read operation takes place as per the design.

## Assumptions

1. I2c module: Contains the core logic for i2c operations.
2. Top module: Instantiates the i2c module and provides test stimuli.
3. Inputs: rst ,sclk ,sda\_in
4. Output: sda\_out
5. Temporary variables: mem,addr,data,ack.
6. Timing: The code uses a clock signal to synchronize operations.
7. Acknowledgement: It is initialized to 0.
8. Reset: When reset is 1, sda\_out is 0. When reset is 0, the transfer of data and address
9. takes place.
10. Memory array: Stores the address.
11. First, the address is stored in sda\_in.
12. If ack=1, the write operation takes place.
13. Write operation: When addr[7] is equal to 1, the data is written to sda\_in.
14. Read operation: When addr[7] is equal to 0, the data is read from the memory.
15. Waveform: For each posedge of a clock cycle, 1 bit address and data are transferred.

Fig: Timing Diagram



## Components and Tool usage

Questa Sim Tool for Verilog Code

Questa Sim is a comprehensive digital simulation and verification tool developed by Siemens EDA (formerly Mentor Graphics). It is part of the Questa Verification Platform and is widely used in the industry for verifying and validating digital designs written in hardware description languages such as Verilog, VHDL, and System Verilog. Below is an overview of Questa Sim, its features, and how it is used for Verilog code simulation and verification.

Overview of Questa Sim

Questa Sim is a high-performance simulation environment that supports multiple hardware description languages and verification methodologies. It is designed to handle the complexities of modern digital designs, including large-scale systems-on-chip (SoCs) and complex FPGA designs. The tool integrates seamlessly with various verification methodologies, including UVM (Universal Verification Methodology), and supports advanced verification features such as constrained random testing, coverage-driven verification, and assertion-based verification.

Key Features:

* + 1. Multi-Language Support:
* Supports Verilog, VHDL, System Verilog, and mixed-language designs.
* Enables co-simulation with other languages and models.
  + 1. Advanced Debugging Capabilities:
* Interactive waveform viewer for detailed signal inspection.
* Advanced breakpoints, watchpoints, and signal tracing features.
* Source code debugging with support for single-stepping through code.
  + 1. Coverage Analysis:
* Code coverage, functional coverage, and assertion coverage.
* Supports coverage-driven verification to ensure comprehensive testing.
  + 1. UVM and OVM Support:

o Fully supports Universal Verification Methodology (UVM) and Open Verification Methodology (OVM).

o Provides built-in libraries and components for creating reusable and scalable verification environments.

* + 1. Performance Optimization:
* High-speed simulation engine for fast execution of large designs.
* Multi-threaded and distributed simulation to leverage multi-core processors and clusters.
  + 1. Assertion-Based Verification:
* Supports System Verilog assertions (SVA) for formal verification.

* Integrates with formal verification tools to check for design correctness.
  + 1. Integration with Other Tools:
* Seamless integration with design and verification tools from Siemens EDA and other vendors.
* Supports industry-standard interfaces and formats.

Using Questa Sim for Verilog Code

1. Writing Verilog Code:
   * Develop your Verilog modules, test benches, and verification components using any text editor or integrated development environment (IDE).
2. Compiling Verilog Code:
   * Use the Questa Sim compiler to compile Verilog files. The tool checks for syntax errors and generates intermediate files for simulation.
   * Command: vlog <verilog\_files>
3. Running Simulations:
   * Launch simulations to verify the functionality of your Verilog code. You can run simulations interactively or in batch mode.

* Command: vsim <top\_module>

1. Debugging and Waveform Viewing:
   * Use the Questa Sim graphical user interface (GUI) to inspect waveforms, set breakpoints, and debug your design.
   * The waveform viewer allows you to add signals of interest and analyze their behavior over time.
2. Coverage Analysis:
   * Enable coverage collection during simulation runs to assess how thoroughly your design has been tested.
   * Generate coverage reports and identify untested parts of your design.
3. Assertion-Based Verification:
   * Write System Verilog assertions to specify design properties and invariants.
   * Questa Sim checks these assertions during simulation to catch violations and design errors.
4. UVM/OVM-Based Verification:
   * Create sophisticated verification environments using UVM/OVM.
   * Questa Sim provides libraries and utilities to facilitate the creation and management of these environments.

## Individual and Team Contribution

|  |  |  |
| --- | --- | --- |
| **Sl No.** | **Member name** | **Work Done** |
| 1. | Siddharth S | Report Preparation |
| 2. | Sindhushree G B | Report Preparation |
| 3. | Sneha Jenifer B | Code Designing |
| 4. | Sohana M V | PPT Preparation |

Table 1: Individual and team contribution

## Project Planning and Execution

|  |  |
| --- | --- |
| **Date** | **Work Done** |
| 25/6/2024 | Understanding and Analyzing the Problem Statement |
| 27/6/2024 | Designing the code |
| 1/7/2024 | Verification and execution |

Table 2: Project planning and execution

## CHAPTER 4 OUTCOMES

During my internship, I had the opportunity to apply my academic knowledge in a real-world setting, gaining invaluable experience and insight into the practical aspects of my field. This experience has been both enriching and transformative, significantly contributing to my professional and personal growth.

### Technical Outcomes:

1. Interfacing Multiple Devices: I²C allows multiple slave devices to communicate with one or more master devices on a single bus, using unique addresses for each device.
2. Simplicity and Efficiency: The protocol is designed to minimize the number of pins and wires needed for communication, typically requiring just two lines (SDA for data and SCL for the clock).
3. Synchronization: I²C uses a clock signal to synchronize data transmission between the master and slave devices, ensuring reliable communication even at different data rates.
4. Scalability: The protocol supports multiple data rates and can accommodate devices with varying speed requirements, from low-speed to high-speed data transfers.
5. Low Power Consumption: I²C is designed to consume minimal power, making it ideal for battery-powered devices and low-power applications.
6. Error Checking: The protocol includes mechanisms for detecting errors, such as acknowledgment bits and parity checks, to ensure data integrity during transmission.

### Non-Technical Outcomes:

* 1. Verbal and Written Communication: Throughout my internship, I significantly improved my verbal and written communication skills. I regularly presented updates and findings to

My team, which helped me to articulate complex technical concepts clearly and confidently. Additionally, writing detailed documentation for the I2C system enhanced my ability to communicate technical information in a structured and comprehensible manner.

* 1. Personality Development: Working in a professional environment contributed to my personality development. I learned to adapt to different working styles and collaborate effectively with team members from diverse backgrounds. This experience helped me build confidence, resilience, and a proactive attitude towards problem-solving.
  2. Time Management: Balancing multiple tasks and meeting project deadlines required effective time management skills. I developed strategies to prioritize my work, allocate time efficiently, and maintain productivity. This experience has made me more disciplined and organized in managing my responsibilities.
  3. Resource Utilization: I honed my skills in utilizing available resources efficiently. Whether it was leveraging online tools for learning new concepts, seeking guidance from mentors, or optimizing the use of software tools for simulation and testing, I learned to make the most of the resources at my disposal to achieve the best results.

In conclusion, my internship has been a highly rewarding experience, providing me with practical technical skills and significant personal growth. The combination of technical achievements and non- technical development has prepared me well for future professional challenges, and I am confident that the skills and knowledge I have gained will be invaluable in my career.



## References

1. "I2C Bus Specification and User Manual" by NXP Semiconductors:

This is the official documentation provided by the inventor of the I2C protocol, NXP (formerly Philips). It covers the technical specifications, electrical characteristics, and communication protocol details.

1. "The I2C Bus: From Theory to Practice" by Dominique Paret

A comprehensive book that covers both the theoretical and practical aspects of the I2C bus, including examplesand implementation details.

1. "Embedded Systems: Real-Time Interfacing to Arm® Cortex™-M Microcontrollers" by Jonathan W. Valvano This book includes sections on interfacing using I2C, including practical examples with ARM Cortex-M microcontrollers.
2. "I2C Bus: Recent Developments and Applications" by Gerd Claus

A detailed overview of recent advancements and applications of the I2C bus in various embedded systems.

1. Microcontroller Manufacturer's Documentation

Many microcontroller manufacturers provide specific documentation on how to implement I2C communication with their products. Examples include datasheets and application notes from companies like Microchip, STMicroelectronics, Texas Instruments, and Atmel.

1. Online Resources

Microchip Technology's I2C Introduction Adafruit's I2C Guide